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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,557	07/27/2001	Elmar Wagner	P2000,0144	1922

24131 7590 11/18/2004

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EXAMINER	
UBILES, MARIE C	

ART UNIT	PAPER NUMBER
2642	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/917,557	WAGNER, ELMAR	
	Examiner	Art Unit	
	Marie C. Ubiles	2642	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *3 and 6-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/27/01, 1/14/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 3 and 6-7 are objected to because of the following informalities:

- In claim 3, lines 2-3 the limitation "has a frequency" was used, for both the first and second signal, the claim language should be corrected in order to differentiate the signal frequencies.
- In claim 6, lines 2-3 the limitation "differential signal" was used, for both the first and second signal.
- -In claims 6-7, the Applicant claims "said first/second signal input includes two terminals for receiving the first/second signal" and "the first/second input signal that is received by said two terminals of said first/second signal input"; the Examiner believes that the claimed "first/second signal" of those limitations should be renamed in order to differentiate the aforementioned switch input signal (i.e. U1, U2, See Fig. 1) from the switch output signal (or "first/second input signal" fed to the multiplier)(i.e. E1, E2, See Fig 1).

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ray, Jr. (US 4,755,761).

As for claim 1, Ray, Jr. discloses an analog multiplier (element 26-1, See Fig. 4) including a first signal input (or *non-delayed in-phase signal I*) for receiving a first signal (See Col. 7, lines 67-68), a second signal input (or *delayed signal Id*) for receiving a second signal (See Col. 7, lines 67-68), and an output for providing a multiplied signal (or *I.Id*)(See Col. 8, lines 16-18).

As for claim 8, Ray, Jr. et al. discloses –in Fig. 4- a first signal path (elements 11-1 through 22a); a second signal path (elements 11-2 through 22b); a first analog multiplier (element 26-1) located in a first signal path, said first analog multiplier including an output (as seen on output *I.Id*) and two inputs (as seen on input signals I and Id); a second analog multiplier (element 26-2) located in a second signal path, said second analog multiplier including an output (as seen on output *Q.Qd*) and two inputs (as seen on input signals Q and Qd) and a differential node (element 22) connected to said output of said first analog multiplier (element 22a) and to said output of said second analog multiplier (element 22b).

The limitations specifying "...a signal derived from the quadrature component of the signal and for thereby providing a *first/second* signal" may be read on *delayed signal Id* and *delayed quadratured-phased signal Qd*.

While Ray, Jr. discloses the use *switch means 16a-16d* (See Fig. 4); Ray, Jr. lacks the "first switching device for polarity reversal, said first switching device connected to said first switching device connected to said first signal input" and "second

switching device for polarity reversal, said second switching device connected to said second switching device connected to said second signal input".

However, as admitted by the Applicant in page 2, Paragraph 25, it is known that in order to suppress DC voltage offsets in amplifiers, the polarity of both the input and the output signal of the amplifier to be periodically changed over.

Thus, based on the admitted prior art, it would have been obvious to one of ordinary skill in the art to modify Ray's, Jr. system by adding switches that will periodically change the inputted signal polarity and in this manner suppress the voltage offsets that may result in crosstalk.

As for claim 2, the limitations claimed by the Applicant may be read on the use of a flip-flop switch, such element may provide the circuit with a periodic polarity change based on the clock pulse signal of the flip-flop switch.

As for claim 3, the limitation specifying that the first and second signal having a frequency may be read on the use of a *non-delayed in-phase signal I* and *delayed signal Id.* In regards to the claimed "changeover frequency" being "not less than two times a frequency selected from the group consisting of the frequency of the first signal." It is well-known in the art that the theorem states, when converting from an analog signal to digital (or otherwise sampling a signal at discrete intervals), the sampling frequency must be *greater than twice* the highest frequency of the input signal in order to be able to reconstruct the original perfectly from the sampled version.

As for claim 4, the Examiner believes that the limitation specifying "the changeover frequency lies in a range between 4 times and 32 times the largest frequency" is not a critical limitation, and it may be read, for example, on using 4X oversampling through 32X oversampling for symbol clock recovery.

As for claim 5, the limitation specifying "the multiplied signal is a voltage that represents the product of the first signal and the second signal", may be read for example on Fig. 3a (See Col. 6, lines 43-59).

As for claim 6, the limitations claimed by the Applicant are obvious over the well-know fact that differential signals reduce crosstalk and that in order to produce "differential signals" (opposite sign voltage or current) at least two pairs or terminals are needed.

Claim 7 is rejected for the same reasons as claim 1.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kucar (US 5,115,454) teaches a method and apparatus for carrier synchronization and data detection.

Van Waasen et al. (US 6,738,433) teaches a quadricorrelator for a demodulator for frequency-modulated signals.

Kurokami et al. (US 5,790,597) teaches an apparatus and method for interferance compensation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marie C. Ubiles whose telephone number is (703) 305-0684. The examiner can normally be reached on 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ahmad Matar can be reached on (703) 305-4731. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Marie C. Ubiles
November 13, 2004.

BING Q. BUI
PRIMARY EXAMINER